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2811

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4-23-02
R. Butler

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLN. OF: Ito

SERIAL NO.: 09/735,005

FILED: December 12, 2000

FOR: Semiconductor Device Having Dummy Gates...

GROUP: 2811

EXAMINER: T. Tran

DOCKET: NEC 444

The Commissioner of Patents & Trademarks
Washington, D.C. 20231

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In connection with the above-identified application, Applicant hereby attaches U.S. Patent Office Form PTOL-1449, including copies of the prior art references listed therein. These references were cited in the Japanese Office Action dated January 22, 2002 of the underlying Japanese patent application. Enclosed is the Japanese Office Action, together with an English translation of the relevant portions thereof. The claims in the present application are believed to be patentably distinguished over these references.

This information disclosure statement is being made pursuant to the duty of disclosure imposed by law and formulated in 37 CFR 1.56(A). No representation is made that the information thus disclosed in fact constitutes prior art or that it is the closest prior art, inasmuch as 37 CFR 1.56 (A) relies on a materiality concept which depends on subjectivity.

In compliance with the requirements of 37 C.F.R. §1.98(a)(3), as a concise statement of relevance, as it is presently understood by the individual designated in 35 U.S.C. §1.56(c)

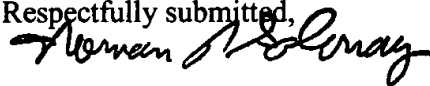
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most knowledgeable about the content of the information, the undersigned attorney of record submits a translation of portions of an official action by a foreign examiner in which the reference was cited. The relevance to the pending U.S. patent application is that the reference was cited in a foreign patent application on the same subject matter. However, no independent analysis of the reference, the accuracy of the statement of the foreign examiner or the claims of the foreign application under the laws of the country or the United States relative to the subject matter claimed in the present application has been made; the present understanding of the contents thereof by the undersigned being based on the translation of the foreign examiner's comments submitted herewith.

The enclosed Information Disclosure Statement is being submitted within three months of the Japanese Office Action, as certified in the attached Certification for Information Disclosure Statement. Therefore, we believe that there are no fees involved with this information disclosure statement. However, in the event there are any fees payable, please charge them to our Deposit Account No. 08-1391.

Respectfully submitted,



Norman P. Soloway
Attorney for Applicant
Reg. No. 24,315

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March 19, 2002 at Manchester, New Hampshire.

By: Kristine Stevens

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**STATEMENT UNDER 37 CFR 1.97(e) ACCOMPANYING
INFORMATION DISCLOSURE STATEMENT**

Docket No.
NEC 444

In Re Application Of: Ito

**COPY OF PAPERS
ORIGINALLY FILED**

Serial No.
09/735,005

Filing Date
December 12, 2000

Examiner
T. Tran

Group Art Unit
2811

Invention: **Semiconductor Device Having Dummy Gates and Its Manufacturing Method**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

This is a statement under the provisions of 37 CFR 1.97(e) in the above-identified application.

Check applicable statement herebelow:

Statement Under 37 CFR 1.97(e)(1)

- ☒ Each item of information contained in the accompanying Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement.

Statement Under 37 CFR 1.97(e)(2)

- ☐ No item of information contained in the accompanying Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned person, after making reasonable inquiry, no item of information contained in the accompanying Information Disclosure Statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

Norman P. Soloway

Signature

Dated: 3/19/02

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Certificate of Mailing by First Class Mail

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1/2

Record ~~(REDACTED)~~ Refer to the List of Cited Documents for the Cited Documents)

- Claims 1~5, 6~7, 8~10
- Reason Number 1, 2
- Cited Documents 1, 2, 3
- Remarks

Please refer to Cited Document 1, especially Figure No. 1~Figure No. 3 and the passages explaining the figures, and to Cited Document 2, especially Figure No. 1, Figure No. 2 and the passages explaining the figures, for formation of a dummy gate after establishing a dummy area in an isolation area.

Please refer to Cited Document 3, especially Figure No. 4 and the passages explaining the figures, for formation of a pattern by partitioning a dummy area pattern and a dummy gate pattern with a component area pattern.

List of Cited Documents

1. Publication of Japanese Laid-Open Patent No. H11-087657
2. Publication of Japanese Laid-Open Patent No. H10-200109
3. Publication of Japanese Laid-Open Patent No. H9-115905

Prior Art Reference Search Result Record

- Searched Fields IPC 7th Edition H01L21/8234
 H01L27/088
 H01L21/822
 H01L27/04
- Prior Art References
 Publication of Japanese Laid-Open Patent No. H11-214634

This prior art reference search result record is without the formation of rejection reasons.

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Remarks

The applicant states in the Written Opinion, cited in the above-mentioned Rejection Reasons, that in the respective cited documents there is no disclosure of either a dummy region by "technology with formation in a plurality of islands that are positioned in parallel to a trench with insulating material imbedded" like in the present application invention or "maintaining smoothing properties when forming things like a dummy region and an element isolating region by a CMP method is difficult".

However, formation of dummy region of a plurality of islands that are positioned in parallel to an imbedded trench in insulation material is conventional technology for maintaining the smoothing properties when trench element isolation is formed by a CMP method, (If necessary, please refer to ones like the Publication of Japanese Laid-Open Patent No. H10-092921 [in particular, Figure No. 6, Figure No. 7] and the Publication of Japanese Laid-Open Patent No. H9-181159 [in particular, Figure No. 1, Figure No. 2.]); thus, the statements of the applicant do not apply because specific complexity cannot be recognized for one skilled in the art for the combining of the above-mentioned conventional technology for maintaining smoothing properties in a CMP method for an invention as described in the respective cited documents that are cited in the above-mentioned Rejection Reasons.

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